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13. ABSTRACT (Maximum 200 words)

This project investigated novel design methodologies for low-energy VLSI circuits and systems. It focused on energy-recovering circuit architectures, a promising alternative to conventional digital CMOS circuits for low-energy operation. It also explored technologies for designing low-energy conventional CMOS circuits.

The main contribution of our research was the discovery of TSEL, the first true single-phase energy-recovering circuit family. TSEL achieves very efficient operation in comparison with conventional CMOS and other energy-recovering circuits. Due to its extremely simple clocking requirements, TSEL is ideal for high-speed design. Moreover, TSEL gates are straightforward to cascade and are thus particularly suitable for the design of energy-efficient datapath components with regular structures.

In the course of this project, we designed, developed, and evaluated layouts of several arithmetic units in TSEL, CMOS and several other energy-recovering logic families. Our designs included 8-bit energy-recovering multipliers, 8-bit carry-lookahead adders, and an 8-point/4-bit Hadamard Transform module. In layout simulations with 0.5μm standard CMOS process parameters, our TSEL designs function for operating frequencies in excess of 200MHz. At 80MHz, they are as energy-efficient as any other energy-recovering alternative and about 5 times more energy-efficient than conventional CMOS. At 200MHz, our TSEL designs are 2 times more efficient than corresponding designs in other energy-recovering logic styles and about 4 times more efficient than conventional static CMOS.

This project has interacted with the ``Low Energy Electronics Design for Mobile Platforms" MURI project currently under way at the EECS Department of the University of Michigan, focusing on the identification of digital signal processing and communication circuitry that is amenable to low-energy implementations using our novel circuit technology.

14. SUBJECT TERMS

low-energy electronic design, low-power electronic design, energy-recovering circuits, adiabatic circuits, VLSI, true single-phase dynamic logic, retiming, edge-triggered circuits, level-clocked circuits, flip-flops, latches, power estimation, power macromodels

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Technologies for Low-Power VLSI Design

Final Progress Report

Prof. Marios C. Papaefthymiou, Principal Investigator

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1 Statement of the problems studied

This project has investigated novel design methodologies for low-energy VLSI circuits and systems. Its primary focus has been on energy-recovering (a.k.a. adiabatic) circuit architectures. By steering currents across low voltage drops and by recycling undissipated energy, these circuits can potentially achieve significantly more efficient operation than conventional digital circuits. Early investigations into adiabatic circuits have yielded very complex designs that are impractical for high-speed design. The main objective of this project has been the discovery of extremely simple energy-recovering circuits which can achieve very high energy efficiency at relatively high operating frequencies.

In addition to energy-recovering circuits, this project has also explored approaches for low-energy conventional CMOS design. This task focused on the development of circuit optimizations that can be used to automatically improve the energy efficiency of any given design.

2 Summary of the most important findings

The main contribution of our research was the discovery of TSEL, the first true single-phase energy-recovering circuit family [7]. TSEL achieves very efficient operation in comparison with conventional CMOS and other adiabatic circuit families. Due to its extremely simple clocking requirements, TSEL is ideal for high-speed design. Moreover, TSEL gates are straightforward to cascade and are thus particularly suitable for designing energy-efficient datapath components with regular structures.

Several adiabatic logic families have been proposed in recent years. Contrary to TSEL, they all require at least two-phase clocks to control cascades. A scheme with asymptotically zero dissipation that requires reversible computations was described in [17]. Two relatively simple energy-recovering logic styles that use diodes to avoid reversibility were proposed in [6, 11]. Complementary adiabatic MOS (CAMOS) and fully adiabatic MOS (ADMOS) were proposed in [5] for high-speed design. Various adiabatic circuit families were introduced and evaluated in [9, 12, 14, 15, 16], including 2N-2P, 2N-2N2P, pass-transistor adiabatic logic (PAL), and clocked CMOS logic (CAL). A 16-bit microprocessor that relies on clock-powered logic to reduce energy consumption has been described in [1, 2].

TSEL is a partially adiabatic logic akin to 2N-2P, 2N-2N2P, and CAL. Power is supplied to TSEL gates by a single-phase clock. Cascades are composed of alternating PMOS and NMOS-type gates. Two DC reference voltages ensure high-speed, high-efficiency operation and enable the cascading of TSEL gates in an NP domino style.

The basic structure of PMOS and NMOS gates in TSEL is shown in Figure 1. The PMOS inverter in Figure 1(a) comprises a pair of cross-coupled transistors (MP_1 and MP_2), a pair of current control switches (MP_3 and MP_4), and two function blocks (MP_5 and MP_6). The port PHI supplies the power clock Φ. The port PREF supplies a constant reference voltage V_{PREF}. Inputs and outputs are dual-rail encoded. The PMOS gate operates in two phases: *discharge* and *evaluate*.

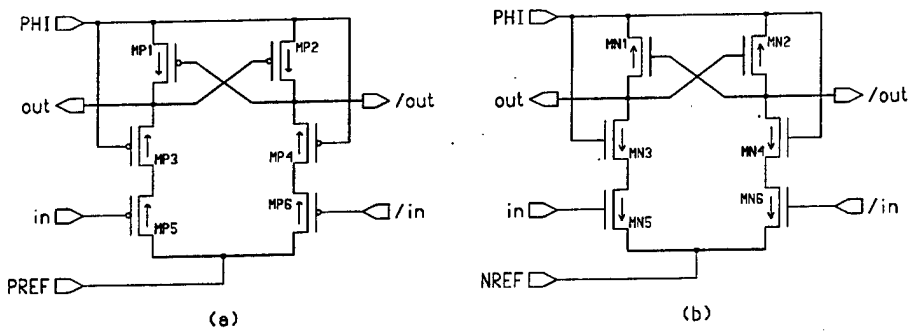


Figure 1: (a) A PMOS and (b) an NMOS inverter in TSEL.

The inverter in Figure 1(b) shows the basic structure of a TSEL NMOS gate. The operation of the NMOS gate is complementary to PMOS and is made up of the two phases *charge* and *evaluate.*

TSEL cascades are built by stringing together alternating PMOS and NMOS gates. The only signal required for controlling a TSEL cascade is the power clock Φ. A single reference voltage suffices to ensure correct operation. The speed and energy-efficiency of the cascade can be improved, however, by using separate reference voltages V_{PREF} and V_{NREF} for the PMOS and NMOS gates, respectively. To ensure minimal dissipation, these voltages must be tuned depending on the operating frequency.

In the course of this project, we designed, developed, and evaluated layouts of several arithmetic units in TSEL, CMOS and several other adiabatic logic families [9, 10, 8]. Our designs included 8-bit multipliers, 8-bit carry-lookahead adders, and an 8-point/4-bit Hadamard Transform (HT) module. In layout simulations with 0.5μm standard CMOS process parameters, our TSEL designs function for operating frequencies in excess of 200MHz. At 80MHz, they are as energy-efficient as any other energy-recovering alternative we considered and about 5 times more energy-efficient than conventional CMOS. At 200MHz, our TSEL designs are 2 times more efficient than any other adiabatic alternative and about 4 times more energy-efficient than their conventional static CMOS counterparts.

In this report, we highlight our pipelined 8-point/4-bit one-dimensional HT module, whose basic architecture is shown in Figure 2. This module was chosen in consultation with members of the "Low Energy Electronics Design for Mobile Platforms" MURI project at the EECS Department of the University of Michigan. Hadamard Transform modules are essential components of modern wireless communication devices and are responsible for a significant fraction of a communicator's dissipation, particularly at standby.

Two versions of the HT module were developed: a TSEL-PN module in which the pipeline starts with PMOS-type gates, and a TSEL-NP module in which the pipeline starts with NMOS type gates. Each design comprised 6,768 transistors and was developed in standard 0.5μm CMOS technology. In HSPICE layout simulations, both designs functioned correctly for frequencies exceeding 280MHz with a 3.0V peak power-clock voltage.

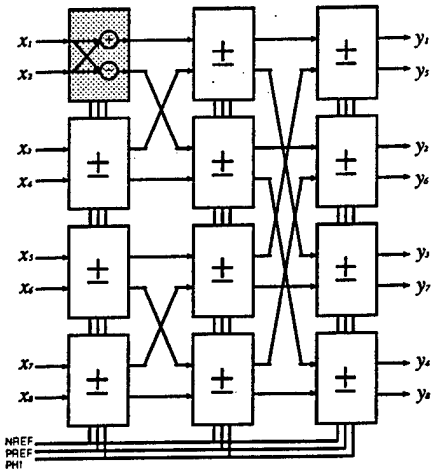
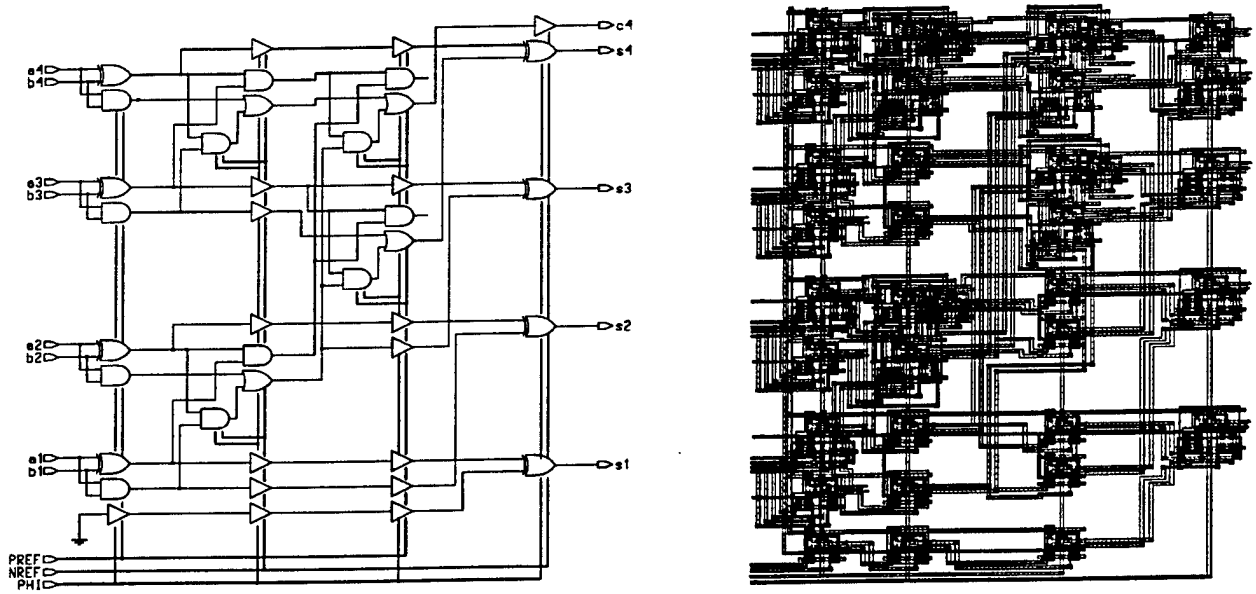


Figure 2: Block diagram of pipelined 8-point Hadamard Transform module. The port PHI supplies the power clock. PREF and NREF are constant reference voltage ports.



(a) (b)

Figure 3: (a) A pipelined 4-bit carry-lookahead adder with stages in the order PNPN. (b) Adder layout in TSEL.

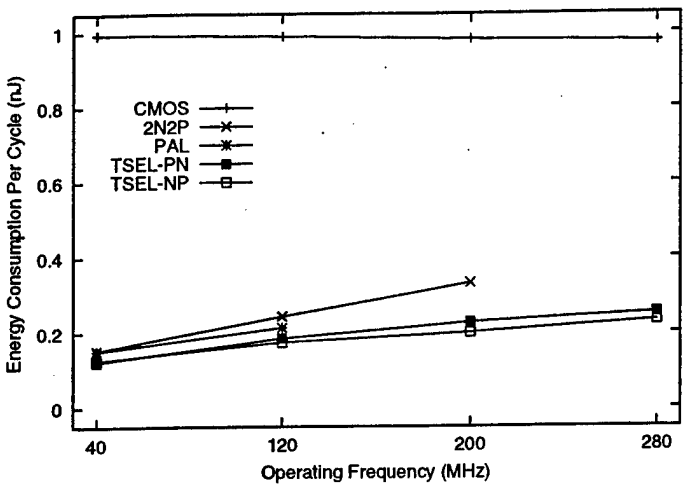


Figure 4: Energy consumption of 8-point HT modules vs. operating frequency.

Each of our HT module consisted of twelve interconnected elementary cells. Each elementary cell comprised two 4-stage pipelined, 4-bit carry-lookahead adders [4]. The netlist and layout of each adder is shown in Figure 3. For driving purposes, the W/L ratio of the cross-coupled latches in each elementary cell was sized to 3.0/0.6. Each transistor in the evaluation trees was sized to 0.9/0.6. To achieve comparable speeds for the PMOS and the NMOS gates in our design, V_{PREF} was set to a larger value than V_{NREF}.

We compared the performance of our TSEL HT modules with corresponding designs in static CMOS and in the adiabatic families 2N-2P and PAL that have a cross-coupled transistor structure similar to TSEL and can be implemented in standard CMOS technology. In our simulations, the power clock was an ideal sinusoid with 100% energy recycling and a peak voltage of 3.0V. All results were obtained using the distributed capacitance and resistance extracted from the layouts of the 8-point HT modules and include the dissipation of the internal clock networks. All primary inputs were driven by typical gate outputs.

Figure 4 gives the per-cycle energy consumption of our designs as a function of their operating frequencies. For the selected W/L ratios, PAL and 2N-2P break down after 120MHz and 200MHz, respectively, due to the short duration of their evaluation phases and the PMOS-only nature of their cross-coupled transistors. As expected, the energy consumption of the static CMOS implementation does not vary with the operating frequency. For operating frequencies above 40MHz, TSEL is less dissipative than every other design. At 200MHz, both TSEL modules are approximately 1.5 times more energy-efficient than 2N-2P. In comparison with their static CMOS counterparts, both TSEL designs are 4 to 5 times more energy-efficient.

Our research activities over the past four yeras extended beyond energy-recovering design to encompass conventional CMOS. In particular, we investigated architectural-level circuit transformations for reducing energy consumption [13]. The main idea behind our technique was to treat each flip-flop as a master-slave pair of level-sensitive latches and transform the original circuit architecture by relocating one of the two

latches. We coined the term *fixed-phase retiming* to describe our optimization. Fixed-phase retiming places latches on interconnections with high capacity and switching activity. Energy dissipation is thus reduced by shielding the high-capacitance node from any switching that occurs during the opaque phase in the operation of the level-sensitive latch. Fixed-phase retiming also reduces energy dissipation by reducing the number of latches in the circuit. We have designed and implemented optimal algorithms that perform fixed-phase retiming while maintaining the functionality of the original circuit. Our algorithms take into account timing constraints for level-sensitive latches and reduce the power dissipation of the original circuits without decreasing their operating frequency.

In addition to power optimization techniques, we commenced the investigation of power macromodeling techniques for sequential CMOS circuits [3]. In the next few years, we expect to expand our research activities in this research area. In particular, we plan to investigate efficient and accurate power macromodeling techniques for programmable systems.

3 List of publications and technical reports

- G. Bernacchia and M. C. Papaefthymiou. Analytical macromodeling for high-level power estimation. Accepted for publication at the *1999 IEEE/ACM International Conference on Computer-Aided Design*, November 1999.

- S. Kim and M. C. Papaefthymiou. Low-energy adder design with a single-phase source-coupled adiabatic logic. Accepted for publication at *PATMOS '99, 9th International Workshop on Power and Timing Modeling, Optimization and Simulation*, October 1999.

- S. Hong, S. Kim, M. C. Papaefthymiou, and W. E. Stark. Low power parallel multiplier design for DSP applications through coefficient optimization. Accepted for publication at the *12th IEEE International ASIC/SOC Conference*, September 1999.

- S. Kim and M. C. Papaefthymiou. Single-phase source-coupled adiabatic logic. Accepted for publication at the *International Symposium on Low-Power Electronics and Design*, August 1999.

- S. Hong, S. Kim, M. C. Papaefthymiou, and W. E. Stark. Power-complexity analysis of pipelined VLSI FFT architectures for low energy wireless communication applications. Accepted for publication at the *42nd Midwest Symposium on Circuits and Systems*, August 1999.

- S. Kim and M. C. Papaefthymiou. Pipelined DSP design with a true single-phase energy-recovering logic style. In *VOLTA '99 IEEE Alessandro Volta International Workshop on Low Power Design*, March, 1999.

- S. Kim and M. C. Papaefthymiou. True single-phase energy-recovering logic for low-power, high-speed VLSI. In *International Symposium on Low-Power Electronics and Design*, August 1998.
- M. C. Knapp, P. J. Kindlmann, and M. C. Papaefthymiou. "Design and Evaluation of Adiabatic Arithmetic Units." *Analog Integrated Circuits and Signal Processing,* Special Issue on "Analog Design Issues in Digital VLSI Circuits and Systems", Vol. 14, pp. 71–79, 1997.
- K. N. Lalgudi and M. C. Papaefthymiou Fixed-Phase Retiming for Low Power Design. In *1996 International Symposium on Low Power Electronics and Design,* August 1996.
- M. C. Knapp, P. J. Kindlmann, and M. C. Papaefthymiou. Implementing and Evaluating Adiabatic Arithmetic Units. In *1996 IEEE Custom Integrated Circuits Conference*, May 1996.

4 List of all participating research personnel

Prof. Marios C. Papaefthymiou, PI

- Promoted to Associate Professor, University of Michigan, June 1999.
- Technical Program Committee Member, *IEEE/ACM International Conference on Computer-Aided Design*, 1996-1998.
- Associate Editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, June 1997–present.
- Associate Editor, *IEEE Transactions on Computers*, June 1999–present.

Suhwan Kim, Graduate Research Assistant

- Achieved PhD candidacy, University of Michigan, December 1998.

Kumar Lalgudi, Graduate Research Assistant

- Received PhD degree in Electrical Engineering, Yale University, January 1997.

Micah Knapp, Graduate Research Assistant

- Received MS degree in Electrical Engineering, Yale University, May 1996.

5 Report of inventions

"True Single-Phase Adiabatic Logic." Patent application No. 60/095,380 filed in the U.S. Patent and Trademark Office on 8/5/98.

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